WE CLAIM:

1. A method for wafer-level assembly of chip-size devices, comprising the steps of:

providing a semiconductor wafer having a plurality of device units, said units having contact pads covered by a solderable metallic member;

providing a wafer-level leadframe having a plurality of segment groups, each group suitable for one of said device units;

connecting said wafer to said leadframe;

encapsulating said assembled wafer and leadframe except for those segment portions intended for external connections; and

singulating said encapsulated assembly into discrete chip-size devices.

2. The method according to Claim 1 wherein said metallic member is a copper stud.

3. The method according to Claim 1 wherein said metallic member is a nickel stud.

4. The method according to Claim 1 wherein said step of connecting is provided by means of solder paste.

5. A method for assembling semiconductor devices, comprising the steps of:

providing a semiconductor wafer having a plurality of device units, said units having an active surface protected by an overcoat, said overcoat having a plurality of windows exposing the metal contact pads, a patterned barrier metal layer on said pad metal in said windows and on portions of said overcoat, which surround the perimeter of said windows, a plurality of patterned metal

studs, one stud each on a barrier layer, each stud having an outer surface suitable to form metallurgical bonds without melting;

providing a leadframe suitable for the whole wafer, said leadframe having a plurality of segment groups, each group suitable for one of said device units, each segment having first and second ends covered by solderable metal;

placing a predetermined amount of solder paste on each of said first segment ends;

aligning said leadframe with said wafer so that each of said paste-covered segment ends is aligned with the corresponding metal stud of the respective device unit;

connecting said leadframe to said wafer by contacting said metal studs and said first segment ends and reflowing said solder paste;

encapsulating said wafer in a molding compound so that said device units and said first segment ends are covered, while said second segment ends remain exposed; and

separating said encapsulated wafer into individual encapsulated device units to create a plurality of assembled, packaged semiconductor devices.

6. The method according to Claim 5 wherein said step of separating said encapsulated wafer comprises a sawing technique.

7. The method according to Claim 5 wherein said step of separating said encapsulated wafer comprises a laser cutting technique.

8. The method according to Claim 5 wherein said device units are integrated circuits.

9. The method according to Claim 5 wherein said assembled, packaged semiconductor devices are chip-scale devices.

10. The method according to Claim 5 further comprising, prior to the step of encapsulating, the step of attaching a metal sheet to the wafer surface opposite to said active device surface so that the sheet surface opposite said attached surface remains exposed after said step of encapsulating.

11. A method for assembling a semiconductor device, comprising the steps of:

providing a semiconductor chip having an active surface protected by an overcoat, said overcoat having a plurality of windows exposing the metal contact pads, a patterned barrier metal layer on said pad metal in said windows and on portions of said overcoat, which surround the perimeter of said windows, a plurality of patterned metal studs, one stud each on a barrier layer, each stud having an outer surface suitable to form metallurgical bonds without melting;

providing a leadframe having a plurality of segments, each segment having first and second ends covered by solderable metal;

placing a predetermined amount of solder paste on each of said first segment ends;

aligning said leadframe with said chip so that each of said paste-covered segment ends is aligned with the corresponding chip metal stud;

connecting said chip to said leadframe by contacting said metal studs and said first segment ends and reflowing said solder paste; and

encapsulating said chip and said first segment ends

by a molding compound, while leaving said second segment ends exposed.

12. The method according to Claim 11 further comprising the step of attaching a heat spreader surface to the chip surface opposite said active surface prior to said step of encapsulating so that the spreader surface opposite said attached surface remains exposed.

13. A semiconductor device comprising:

a semiconductor chip having an active surface protected by an overcoat, said overcoat having a plurality of windows exposing the metal contact pads;

a patterned barrier layer on said pad metal in said windows and on portions of said overcoat, which surround the perimeter of said windows;

a plurality of patterned metal studs, one stud each on a barrier layer, each stud having an outer surface suitable to form metallurgical bonds without melting;

a plurality of leadframe segments, each segment having first and second ends, the first end of each segment connected to one of said studs on said contact pads, respectively; and

said chip and said leadframe segments encapsulated by a molding compound except for the second end of each segment, which remains exposed.

14. The device according to Claim 13 wherein said metal contact pads comprise aluminum or an alloy thereof.

15. The device according to Claim 13 wherein said metal contact pads comprise copper or an alloy thereof.

16. The device according to Claim 13 wherein said barrier layer comprises a titanium/tungsten alloy.

17. The device according to Claim 13 wherein said barrier layer is selected from a group consisting of titanium, tungsten, tantalum, molybdenum, chromium, vanadium, alloys thereof, stacks thereof, and chemical compounds thereof.

18. The device according to Claim 13 wherein said barrier layer has a thickness range from about 10 to 30 nm.

19. The device according to Claim 13 wherein said stud metal comprises copper or an alloy thereof.

20. The device according to Claim 13 wherein said stud metal comprises nickel or an alloy thereof.

21. The device according to Claim 13 wherein said stud has a thickness range from about 20 to 50 μm.

22. The device according to Claim 13 wherein said outer surface of said stud metal provides its ability to form metallurgical bonds without melting by a deposited film, which is selected from a group consisting of a layer of nickel followed by an outermost layer of palladium, a layer of nickel followed by an outermost layer of gold, and a layer of nickel followed by a layer of palladium and an outermost layer of gold.

23. The device according to Claim 22 wherein the thickness of said film is less than 15 nm.

24. The device according to Claim 13 wherein said leadframe segments comprise a base of metal covered by a layer of solderable metal.

25. The device according to Claim 24 wherein said base metal is copper in the thickness range from about 100 to 300 μm, and said solderable metal is nickel in the thickness range from about 0.2 to 1.0 μm.

26. The device according to Claim 13 wherein said first segment ends have an outer region covered by a silver

or palladium layer.

27. The device according to Claim 13 wherein said second segment ends have an outer region covered by a palladium layer.

28. The device according to Claim 13 wherein said overcoat comprises silicon nitride.

29. The device according to Claim 13 wherein said overcoat is selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbide, or a layered stack of said materials.

30. The device according to Claim 13 wherein said segment-to-stud connection is provided by reflowable metal.

31. The device according to Claim 30 wherein said reflowable metal is a solder paste comprising a mixture of flux and one or more of the metals tin, indium, bismuth, silver, and lead, said paste smoothing any uneven surface contour of said patterned stud.

32. The device according to Claim 13 further comprising a heat spreader attached to the chip surface opposite said active surface.